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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/865,200	05/24/2001	Sang-Ryul Park	678-658 (P9451)	3891

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EXAMINER	
CASCHERA, ANTONIO A	
ART UNIT	**PAPER NUMBER**
2628	

DATE MAILED: 08/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/865,200	PARK, SANG-RYUL	
	Examiner	Art Unit	
	Antonio A. Caschera	2628	

-- The MAILING DATE of this communication appears on the c ver sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in the pending application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bodenkamp et al. (U.S. Patent 5,243,447) in view of Mizuyabu et al. (U.S. Patent 6,297,832 B1).

In reference to claims 1 and 4, Bodenkamp et al. discloses prior art frame buffer systems comprising separate graphics and video frame buffers for storing graphics and video data respectively (see column 5, lines 6-10, 22-24 and #21, 22 of Figure 1). Bodenkamp et al. also discloses the graphics data being in the form of RGB type data while the video data in YUV format (see column 5, lines 11-12 and 24-26). Bodenkamp et al. discloses receiving the data from a memory bus connected to an enhanced display controller in his improvement to the prior art system (see column 6, lines 53-55 and #15 and 50 of Figure 4). Bodenkamp et al. also discloses the display controller to comprise of a conversion and dithering unit, which converts video YUV data to the preferred format of RGB (see column 6, lines 59-64 and column 7, lines

57-65). Bodenkamp et al. does not explicitly disclose a timing generator for generating a timing signal for alternatively obtaining access to the first and second memories and providing such a signal to the memories. Mizuyabu et al. discloses a method and apparatus for memory access scheduling in a video graphics system (see column 1, lines 6-8). Mizuyabu et al. discloses a video graphics circuit including a memory comprising of two different banks, a memory controller, a video display engine along with a graphics display engine (see column 3, lines 43-47 and Figure 1). Mizuyabu et al. discloses the memory controller comprising of a scheduler and a sequencer assessing and dealing with timing penalties associated with memory access and issuing the actual commands to access the actual data (see column 5, lines 3-12 and #22, 24 of Figure 1). Note, the Office interprets the memory controller of Mizuyabu functionally equivalent to the timing signal generator of Applicant's claims. Mizuyabu et al. further discloses a merging block which merges graphics and video data and passes the output to a display (see column 3, lines 49-67, #30, 40, 50 and 52 of Figure 1). Note, the Office interprets the combination of the memory controller and merging block of Mizuyabu functionally equivalent to the on-screen-display controller of Applicant's claims since these units in Mizuyabu: a) control the writing/reading of different types of memory to memory banks, b) operate upon graphics and video data and c) combine both graphics and video data for display. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the memory accessing and data merging techniques of Mizuyabu et al. with the graphical/video frame buffer techniques of Bodenkamp et al. in order to provide the important timing demands of graphical and real-time video display systems by avoiding memory access penalties as much as possible, creating a more efficient memory access for the system as a whole (see column 1, lines 29-32,

54-59 and columns 1-2, lines 66-2 of Mizuyabu et al.). Further note, the recitation "A color display driving apparatus in a portable mobile telephone" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

In reference to claim 2, Bodenkamp et al. and Mizuyabu et al. disclose all of the claim limitations as applied to claim 1 above in addition, Bodenkamp et al. also discloses the conversion and dithering unit performing an interpolation of YUV data, to prepare for the YUV-RGB conversion (see column 8, lines 11-16).

In reference to claim 3, Bodenkamp et al. and Mizuyabu et al. disclose all of the claim limitations as applied to claim 1 above. Bodenkamp et al. discloses the graphics data being in the form of RGB type data while the video data in YUV format (see column 5, lines 11-12 and 24-26). Mizuyabu et al. discloses a video graphics circuit including a memory comprising of two different banks, a memory controller, a video display engine along with a graphics display engine (see column 3, lines 43-47 and Figure 1). Mizuyabu et al. further discloses a merging block which merges graphics and video data and passes the output to a display (see column 3, lines 49-67, #30, 40, 50 and 52 of Figure 1).

In reference to claim 5, Bodenkamp et al. and Mizuyabu et al. disclose all of the claim limitations as applied to claim 1 above. Bodenkamp et al. discloses the graphics data being in

the form of RGB type data while the video data in YUV format (see column 5, lines 11-12 and 24-26). Bodenkamp et al. also discloses the display controller to comprise of a conversion and dithering unit, which converts video YUV data to the preferred format of RGB (see column 6, lines 59-64 and column 7, lines 57-65). Mizuyabu et al. discloses the memory controller comprising of a scheduler and a sequencer assessing and dealing with timing penalties associated with memory access and issuing the actual commands to access the actual data (see column 5, lines 3-12 and #22, 24 of Figure 1). Note, the Office interprets the memory controller of Mizuyabu et al. to inherently provide graphics and video data to the graphics display engine and video display engine in "latches" since Mizuyabu et al. discloses the memory being of SDRAM or synchronous dynamic random access memory type which utilizes a clock signal to output data as do the latches of Applicant's claims (see Figure 1 of Applicant's Drawings).

Response to Arguments

3. Applicant's arguments filed 06/08/06 have been fully considered but they are not persuasive.

In reference to claims 1-5, Applicant argues that Bodenkamp et al. does not disclose an OSD controller combining RGB data, which is YUV data output from the first memory and converted, and RGB data of the second memory, and then outputting the combined data to the display unit (see page 3, 4th paragraph of Applicant's Remarks). Applicant further states, "...Examiner stated that Bodenkamp et al. disclosed all of the limitation of the claims except for a timing generator that allegedly is disclosed by Mizuyabu et al." (see page 2, 1st paragraph of Applicant's Remarks).

Firstly, the Office has clearly stated that Bodenkamp et al. does not disclose the timing generator of the Applicant's claims and has clearly relied upon and shown that Mizuyabu et al. discloses such an element along with a functionally equivalent to the OSD controller element of Applicant's claims (see above rejection of claims 1 and 4, specifically pages 2-3 of this Office Action). Therefore the above statement, that the Examiner relies upon Bodenkamp et al. to disclose all of the limitations except for the timing generator, is incorrect.

Secondly, Bodenkamp et al. explicitly discloses utilizing two frame buffers for storing graphics and video data separately (see column 5, lines 6-10, 22-24 and #21, 22 of Figure 1). Bodenkamp et al. also discloses the display controller to comprise of a conversion and dithering unit, which converts video YUV data to the preferred format of RGB (see column 6, lines 59-64 and column 7, lines 57-65). These teachings combined with the teachings of Mizuyabu et al., who discloses a memory controller comprising of a scheduler and a sequencer along with a merging block which merges graphics and video data and passes the output to a display (see column 3, lines 49-67, column 5, lines 3-12 and #22, 24, 30, 40, 50 and 52 of Figure 1), disclose all of the claim limitations as recited by Applicant's claims.

Further, Applicant seems to suggest that claims 1 and 4 disclose the OSD controller "including" the timing signal generator (see page 2, 4th paragraph of Applicant's Remarks). The Office notes that such is not the case, as the claims nowhere suggest such a configuration. It is noted that the features upon which applicant relies (i.e., the OSD controller "including" the timing signal generator) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Antonio Caschera whose telephone number is (571) 272-7781. The examiner can normally be reached Monday-Thursday and alternate Fridays between 7:00 AM and 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung, can be reached at (571) 272-7794.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

571-273-8300 (Central Fax)

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (571) 272-2600.

aac
8/10/06

PATENT EXAMINER

KEE M. TUNG
SUPERVISORY PATENT EXAMINER